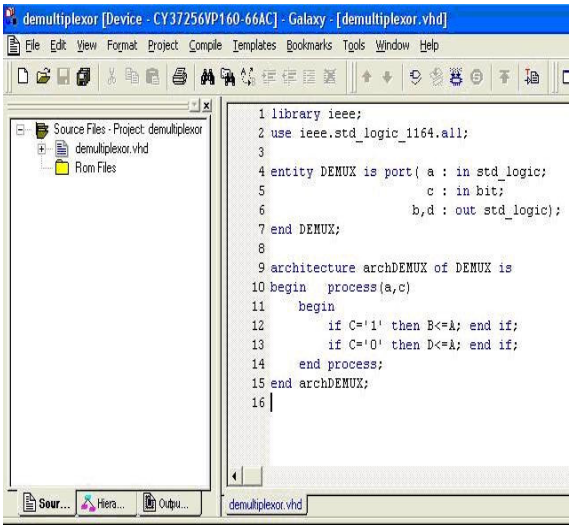
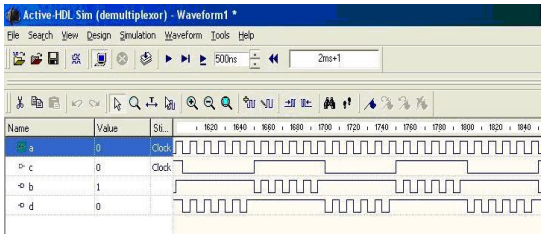
Example 3. Design, simulation, programming and test of a demultiplexer in LEDVCC

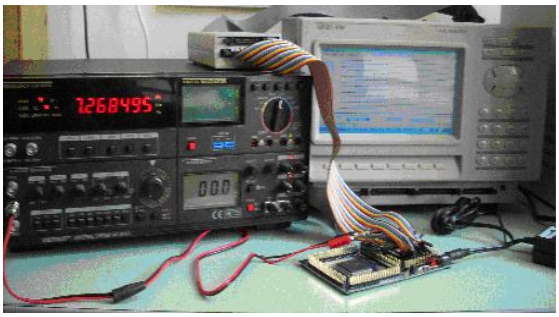


VHDL description of the demultiplexor

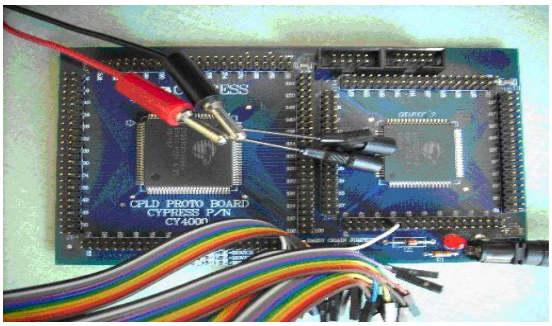


Simulation results in ACTIVE-Sim for the demultiplexer

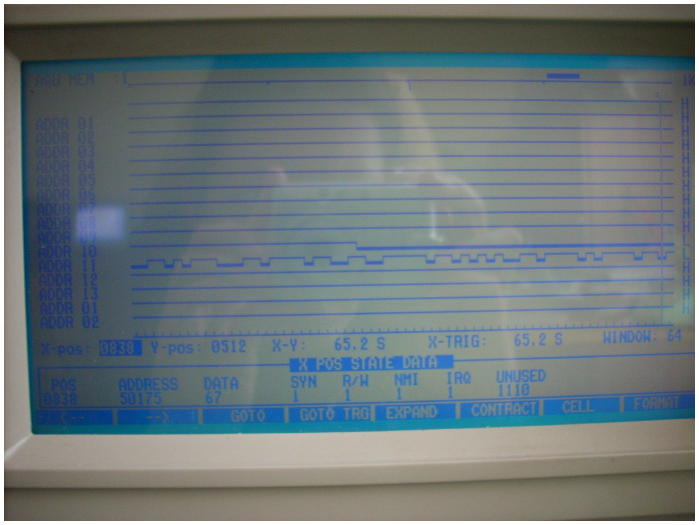
Programming the demultiplexer on the CPLD CY37256VP160-66AC in ISR



Pulse generator and logic analyzer connected to the CYPRESS board with the programmed demultiplexor on the CPLD



Connection of the cables to the Cypress board



Waveforms on the logic analyzer screen