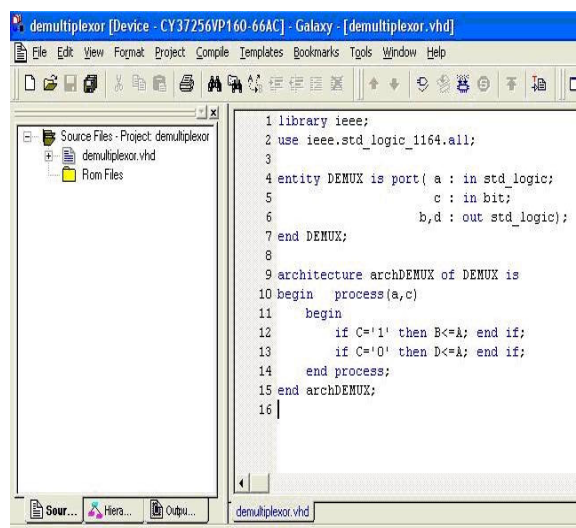
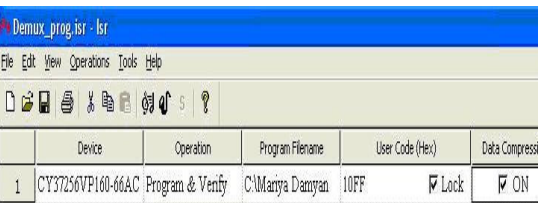
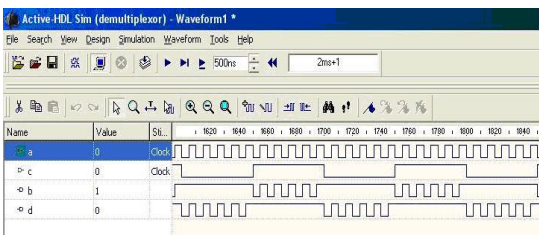


Example 3. Design, simulation, programming and test of a demultiplexer in LEDVCC



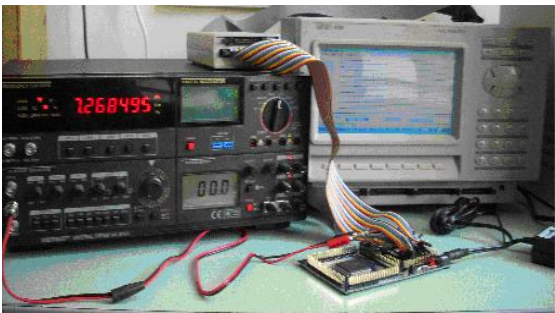
```
1 library ieee;
2 use ieee.std_logic_1164.all;
3
4 entity DEMUX is port( a : in std_logic;
5                      c : in bit;
6                      b,d : out std_logic);
7 end DEMUX;
8
9 architecture archDEMUX of DEMUX is
10 begin
11   process(a,c)
12   begin
13     if C='1' then B<=a; end if;
14     if C='0' then D<=a; end if;
15   end process;
16 end archDEMUX;
```

VHDL description of the demultiplexer

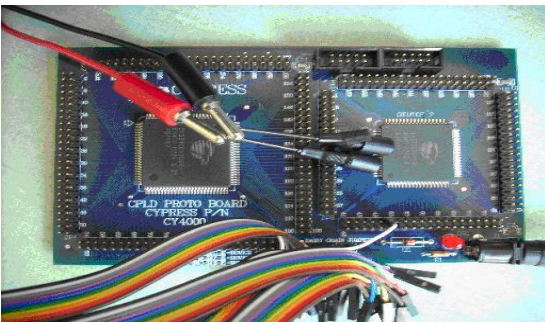


| | Device | Operation | Program Filename | User Code (Hex) | Data Compress |
|---|-------------------|------------------|---------------------|-----------------|---|
| 1 | CY37256VP160-66AC | Program & Verify | C:\Mariya Damianova | 10FF | <input checked="" type="checkbox"/> Lock <input checked="" type="checkbox"/> ON |

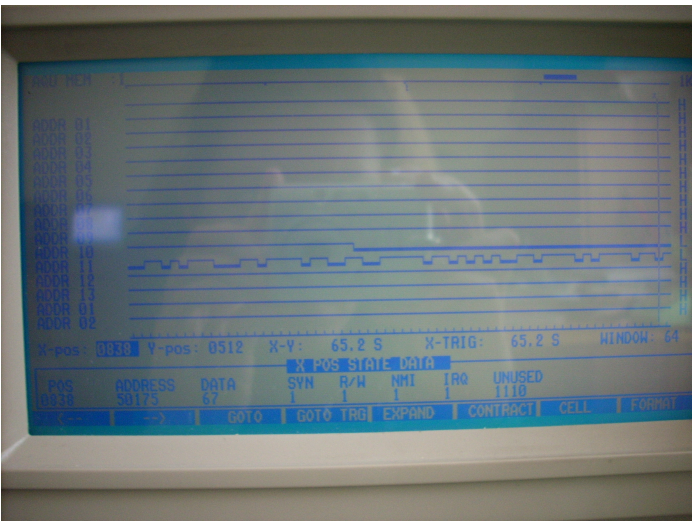
Programming the demultiplexer on the CPLD CY37256VP160-66AC in ISR



Pulse generator and logic analyzer connected to the CYPRESS board with the programmed demultiplexer on the CPLD



Connection of the cables to the Cypress board



Waveforms on the logic analyzer screen