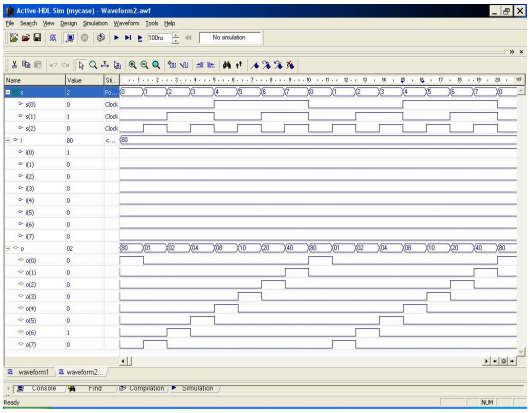
Example 1. Rotation of 8-bit vector using CASE in the VHDL description

```
library ieee;
use ieee.std_logic_1164.all;

entity Rot_shifter is port(s :in bit_vector(0 to 2);
  i :in bit_vector(0 to 7);
  o :out bit_vector(0 to 7));
end Barrel_shifter;

architecture demo of Rot_shifter is
  begin process (s, i)
     begin
        case s is
           WHEN "000"=>
              o<=i;
              WHEN "001"=>
                 o<=(i(1),i(2),i(3),i(4),i(5),i(6),i(7),i(0));
              WHEN "010"=>
                 o<=(i(2),i(3),i(4),i(5),i(6),i(7),i(0),i(1));
              WHEN "011"=>
                 o<=(i(3),i(4),i(5),i(6),i(7),i(0),i(1),i(2));
              WHEN "100"=>
                 o<=(i(4),i(5),i(6),i(7),i(0),i(1),i(2),i(3));
              WHEN "101"=>
                 o<=(i(5),i(6),i(7),i(0),i(1),i(2),i(3),i(4));
              WHEN "110"=>
                 o<=(i(6),i(7),i(0),i(1),i(2),i(3),i(4),i(5));
              WHEN "111"=>
                 o<=(i(7),i(0),i(1),i(2),i(3),i(4),i(5),i(6));
           end case;
      end process;
```

VHDL description of 8-bit rotation with CASE



Simulation results in ACTIVE-Sim

s	o
000	10000000
001	00000001
010	00000010
011	00000100
100	00001000
101	00010000
110	00100000
111	01000000

Simulation results in a table